WHAT IS CLAIMED IS:

1. A printed circuit board (PCB) structure usable in a connector for reducing crosstalk, the PCB structure comprising:

at least one PCB, the PCB including a plurality of substrates and a plurality of metalized layers between the substrates, the substrates including at least one first substrate made of a first material and at least one second substrate made of a second material, the first material having a first dielectric constant, the second material having a second dielectric constant lower in rate of decline with frequency than the first dielectric constant;

at least one first capacitor provided on the at least one first substrate at a first stage area of the PCB structure; and

at least one second capacitor provided on the at least one second substrate at a second stage area of the PCB structure.

2. The PCB structure of claim 1, wherein the first dielectric constant is about 4.0 at 1MHz with a rate of decline being 0.4 per decade of frequency between 1MHz and 1GHz.

3. The PCB structure of claim 1, wherein the second dielectric constant is about 4.0 and remains constant across a frequency range of 1MHz and 1GHz.

4. The PCB structure of claim 1, wherein the substrates of the PCB are five substrates stacked on each other,

a first one, a second one, and a portion of a third one of the substrates are made of the second material, and

a portion of the third one, a fourth one, and a fifth one of the substrates are made of the first material.

5. The PCB structure of claim 4, wherein the at least one first capacitor includes two first capacitor components formed on the fourth one and fifth one of the substrates at the first stage area of the PCB structure.

6. The PCB structure of claim 5, wherein the two first capacitor components are interdigital capacitors or plates of a parallel plate capacitor.

7. The PCB structure of claim 4, wherein the at least one second capacitor includes two second capacitor components formed on the second one and third one of the substrates at the second stage area of the PCB structure.

8. The PCB structure of claim 7, wherein the two second capacitor components are interdigital capacitors or plates of a parallel plate capacitor.

9. The PCB structure of claim 1, wherein the substrates of the PCB are four substrates stacked on each other,

a first one and a second one of the substrates are made of the first material, and

a third one and a fourth one of the substrates are made of the second material.

10. The PCB structure of claim 9, wherein the at least one first capacitor includes a first capacitor formed on the second one of the substrates at the first stage area of the PCB structure.

11. The PCB structure of claim 9, wherein the at least one second capacitor includes a second capacitor formed on the fourth one of the substrates at the second stage area of the PCB structure.

12. The PCB structure of claim 1, wherein the at least one PCB includes first and second PCBs, the first PCB including substrates made of the first material, the second PCB including substrates made of the second material.

13. The PCB structure of claim 12, wherein the at least one first capacitor includes two first capacitor components formed on at least two of the substrates of the first PCB at the first stage area of the PCB structure.

14. The PCB structure of claim 13, wherein the two first capacitor components are interdigital capacitors or plates of a parallel plate capacitor.

15. The PCB structure of claim 12, wherein the at least one second capacitor includes two second capacitor components formed on at least two of the substrates of the second PCB at the second stage area of the PCB structure.

16. The PCB structure of claim 15, wherein the two second capacitor components are interdigital capacitors or plates of a parallel plate capacitor.

17. A printed circuit board (PCB) structure usable in a connector for reducing crosstalk, the PCB structure comprising:

a printed circuit board (PCB) including a plurality of substrates stacked up and a plurality of metalized layers between the substrates, the substrates being made of a material with a dielectric constant having a high rate of decline with frequency;

at least one first capacitor provided on one of the substrates at a first stage area of the PCB structure; and

at least one second capacitor provided on one of the substrates at a second stage area of the PCB structure.

18. The PCB structure of claim 17, wherein the substrate material has a dielectric constant of about 4.0 at 1MHz with a rate of decline being 0.4 per decade of frequency between 1MHz and 1GHz.

19. The PCB structure of claim 17, wherein the at least one first capacitor includes two first capacitor components formed on at least two of the substrates at the first stage area of the PCB structure.

20. The PCB structure of claim 19, wherein the two first capacitor components are interdigital capacitors or plates of a parallel plate capacitor.

21. The PCB structure of claim 17, wherein the at least one second capacitor includes a separate second discreet capacitor surface-mounted on a first one or under a last one of the substrates at the second stage area of the PCB structure.

22. A connector for reducing crosstalk, comprising:

at least one printed circuit board (PCB), the PCB including a plurality of substrates and a plurality of metalized layers between the substrates, the substrates including at least one first substrate made of a first material and at least one second substrate made of a second material, the first material having a first dielectric constant, the second material having a second dielectric constant lower in rate of decline with frequency than the first dielectric constant;

at least one first capacitor provided on the at least one first substrate at a first stage area of the connector;

at least one second capacitor provided on the at least one second substrate at a second stage area of the connector; and

at least one conductive contact provided on the PCB.

23. The connector of claim 22, wherein the first dielectric constant is about 4.0 at 1MHz with a rate of decline being 0.4 per decade of frequency between 1MHz and 1GHz.

24. The connector of claim 22, wherein the second dielectric constant is about 4.0 and remains constant across a frequency range of 1MHz and 1GHz.

25. The connector of claim 22, wherein the substrates of the PCB are five substrates stacked on each other,

a first one, a second one, and a portion of a third one of the substrates are made of the second material, and

a portion of the third one, a fourth one, and a fifth one of the substrates are made of the first material.

26. The connector of claim 25, wherein the at least one first capacitor includes two first capacitor components formed on the fourth one and fifth one of the substrates at the first stage area of the connector.

27. The connector of claim 25, wherein the at least one second capacitor includes two second capacitor components formed on the second one and third one of the substrates at the second stage area of the connector.

28. The connector of claim 22, wherein the substrates of the PCB are four substrates stacked on each other,

a first one and a second one of the substrates are made of the first material, and

a third one and a fourth one of the substrates are made of the second material.

29. The connector of claim 28, wherein the at least one first capacitor includes a first capacitor formed on the second one of the substrates at the first stage area of the connector.

30. The connector of claim 28, wherein the at least one second capacitor includes a second capacitor formed on the fourth one of the substrates at the second stage area of the connector.

31. The connector of claim 22, wherein the at least one PCB includes first and second PCBs, the first PCB including substrates made of the first material, the second PCB including substrates made of the second material.

32. The connector of claim 31, wherein the at least one first capacitor includes two first capacitor components formed on at least two of the substrates of the first PCB at the first stage area of the connector.

33. The connector of claim 31, wherein the at least one second capacitor includes two second capacitor components formed on at least two of the substrates of the second PCB at the second stage area of the connector.

34. A connector for reducing crosstalk, comprising:

a printed circuit board (PCB) including a plurality of substrates stacked up and a plurality of metalized layers between the substrates, the substrates being made of a material with a dielectric constant having a high rate of decline with frequency;

at least one first capacitor provided on one of the substrates at a first stage area of the connector;

at least one second capacitor provided on one of the substrates at a second stage area of the connector; and

at least one conductive contact provided on the PCB.

35. The connector of claim 34, wherein the substrate material has a dielectric constant of about 4.0 at 1MHz with a rate of decline being 0.4 per decade of frequency between 1MHz and 1GHz.

36. The connector of claim 34, wherein the at least one first capacitor includes two first capacitor components formed on at least two of the substrates at the first stage area of the connector.

37. The connector of claim 36, wherein the two first capacitor components are interdigital capacitors or plates of a parallel plate capacitor.

38. The connector of claim 34, wherein the at least one second capacitor includes a separate second discreet capacitor surface-mounted on a first one or under a last one of the substrates at the second stage area of the connector.